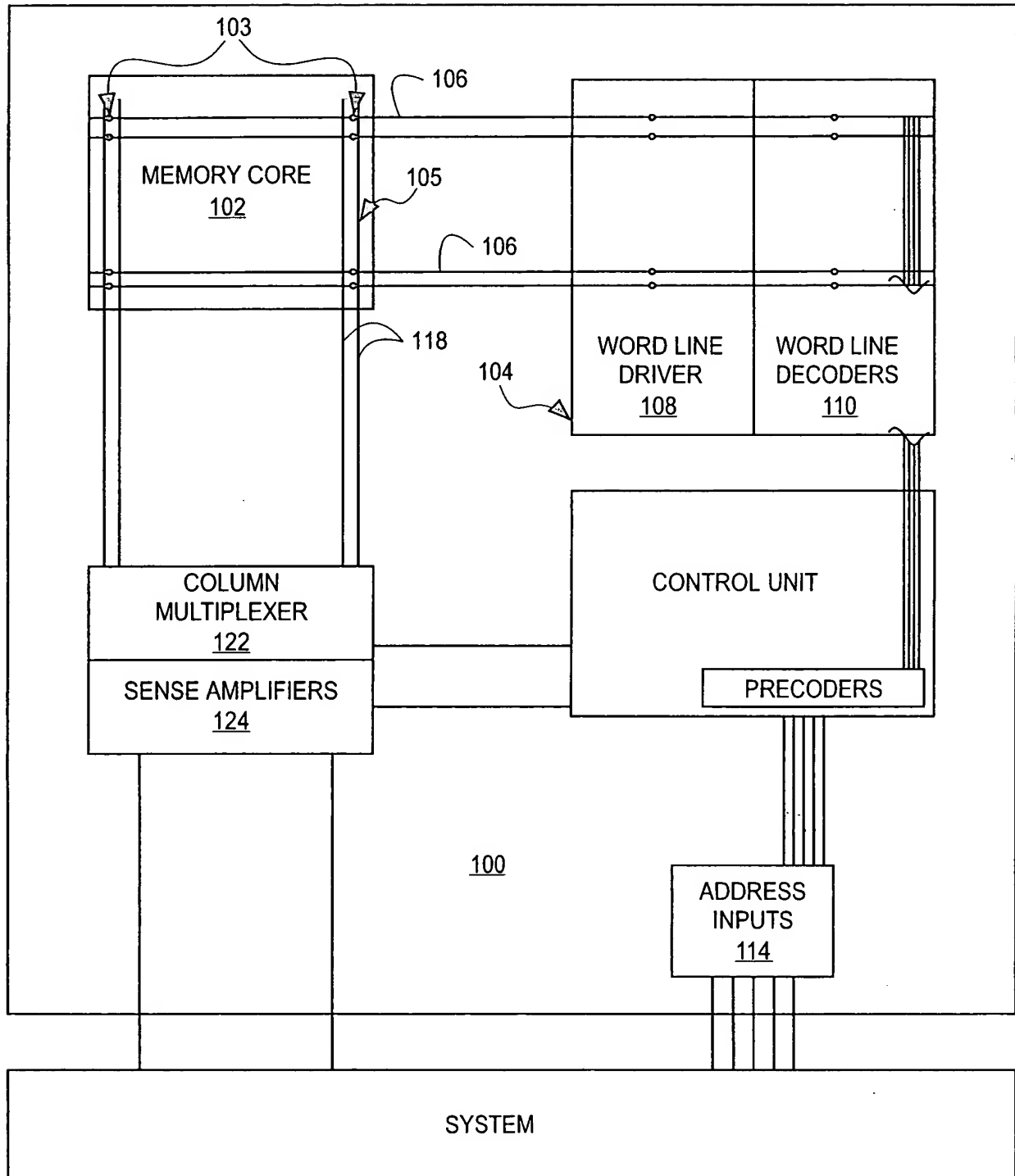


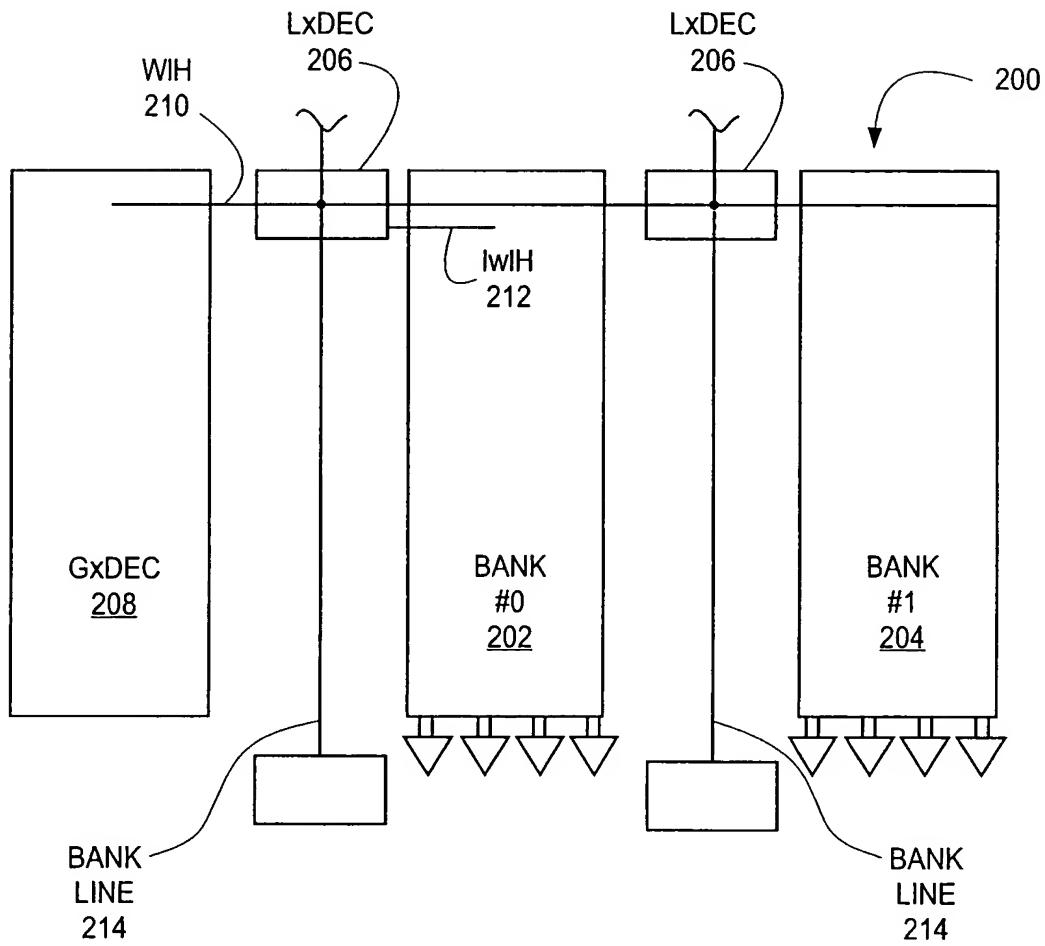
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FIG. 1



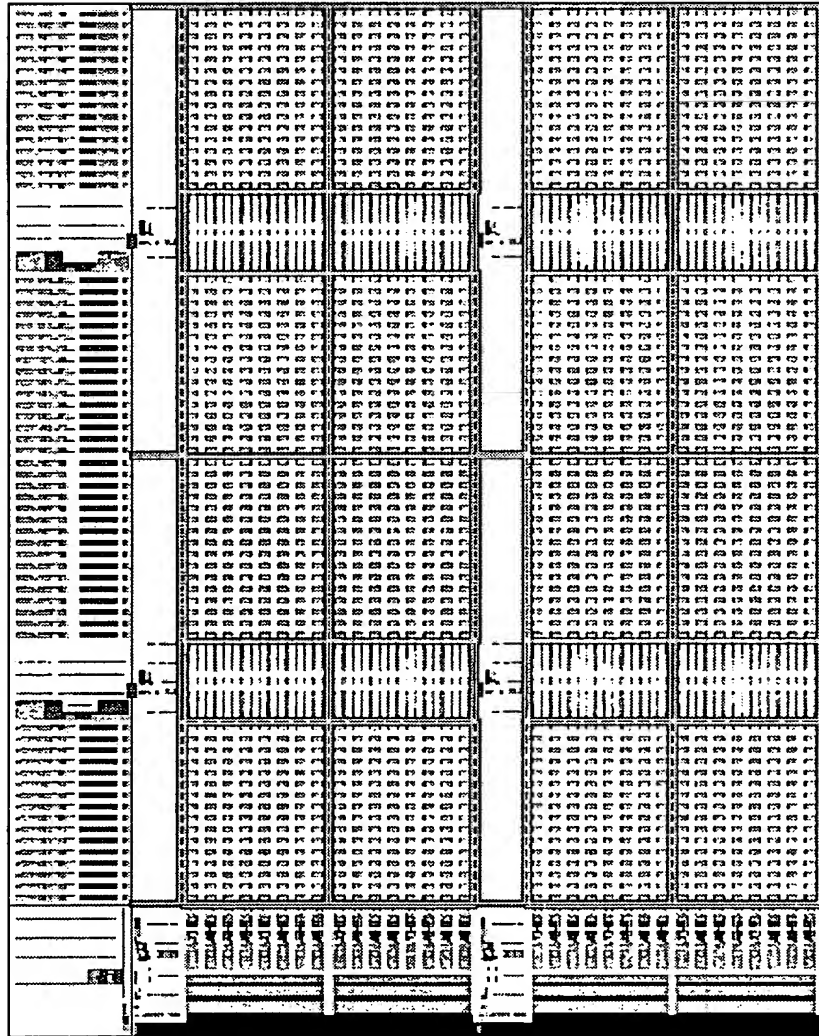
2/26

FIG. 2



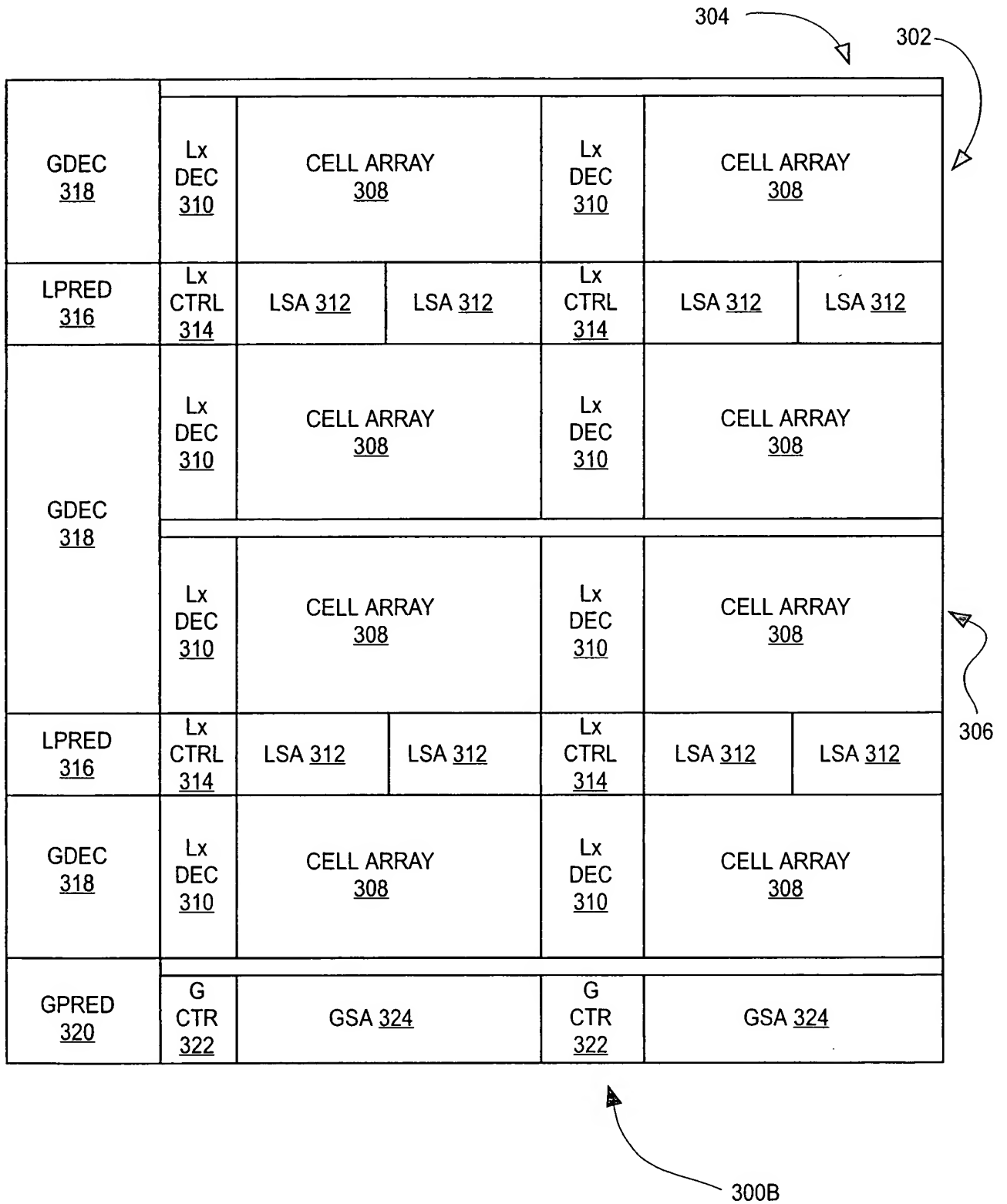
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FIG. 3A



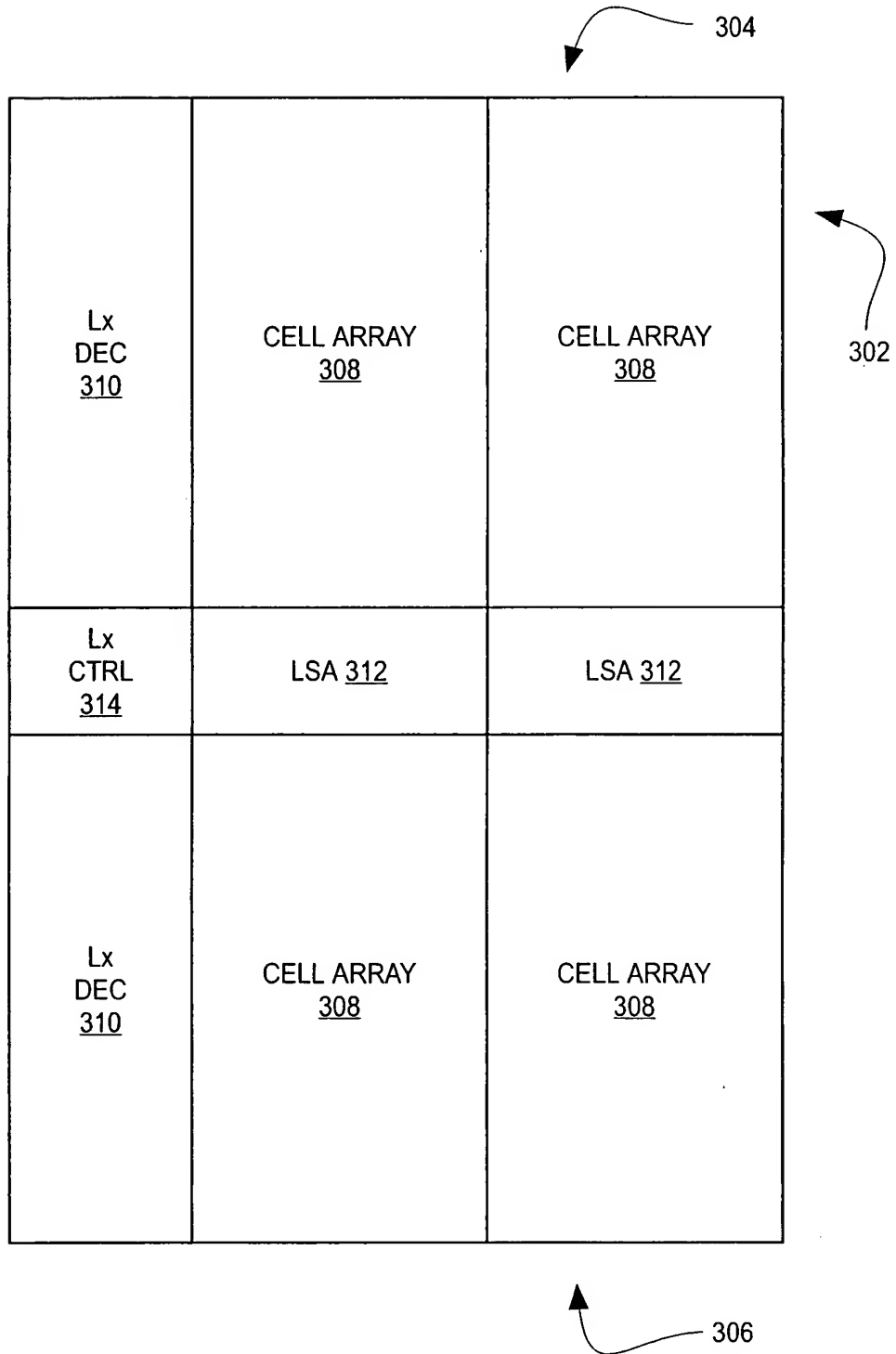
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FIG. 3B



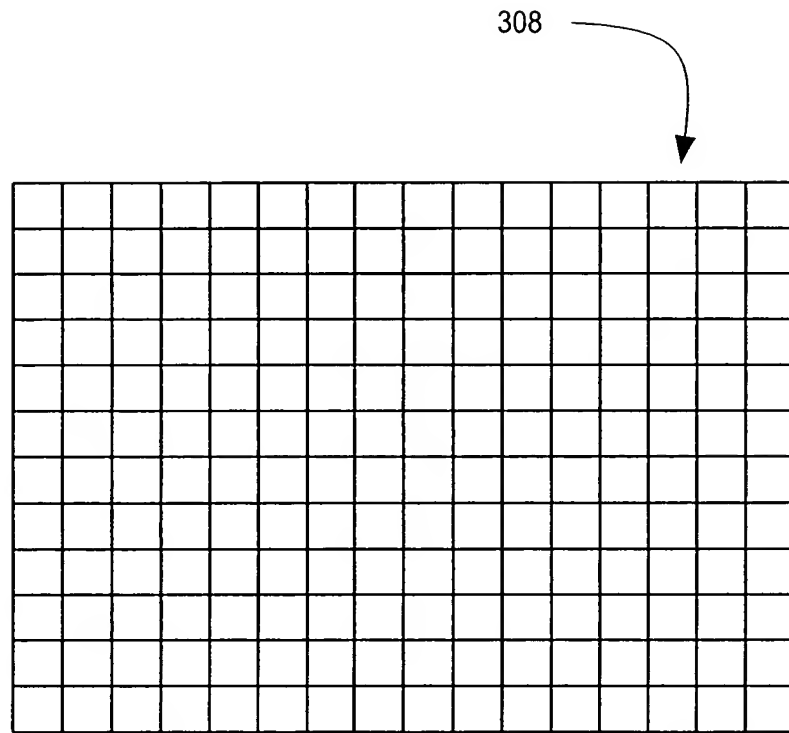
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FIG. 4



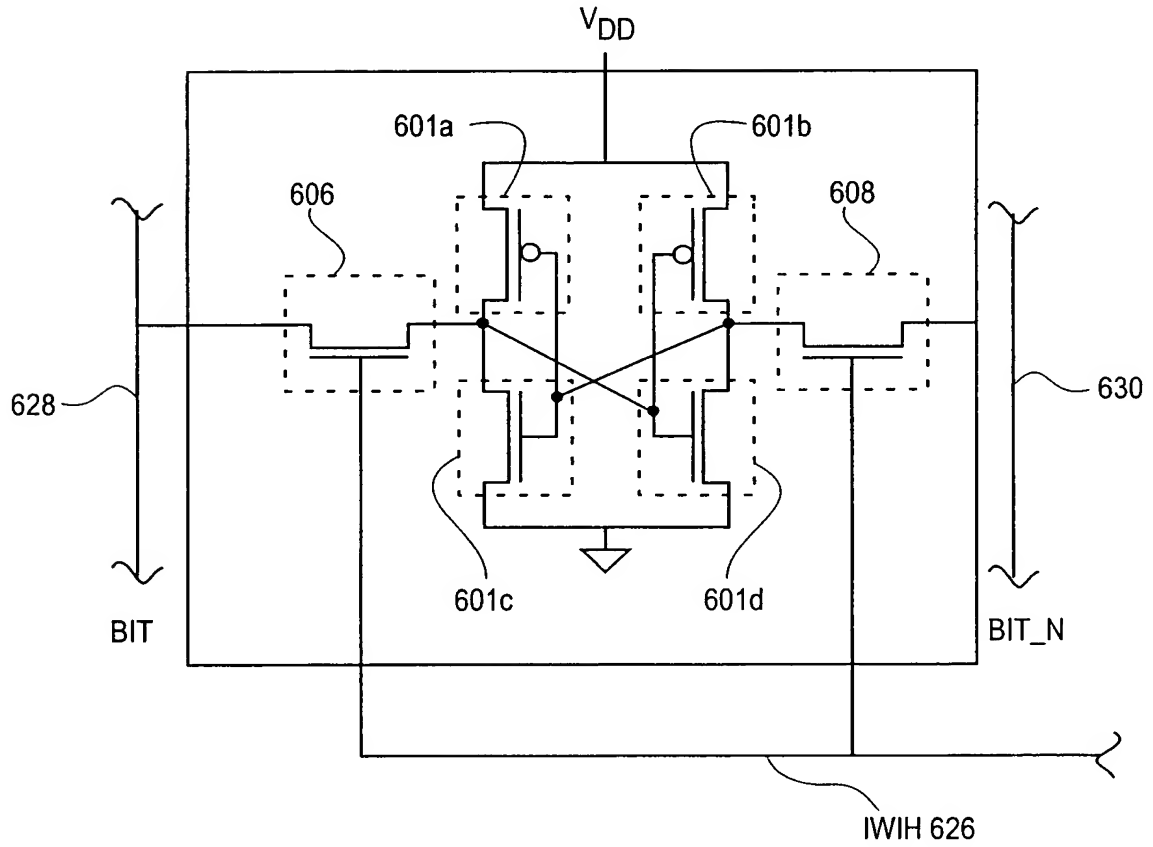
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**FIG. 5**

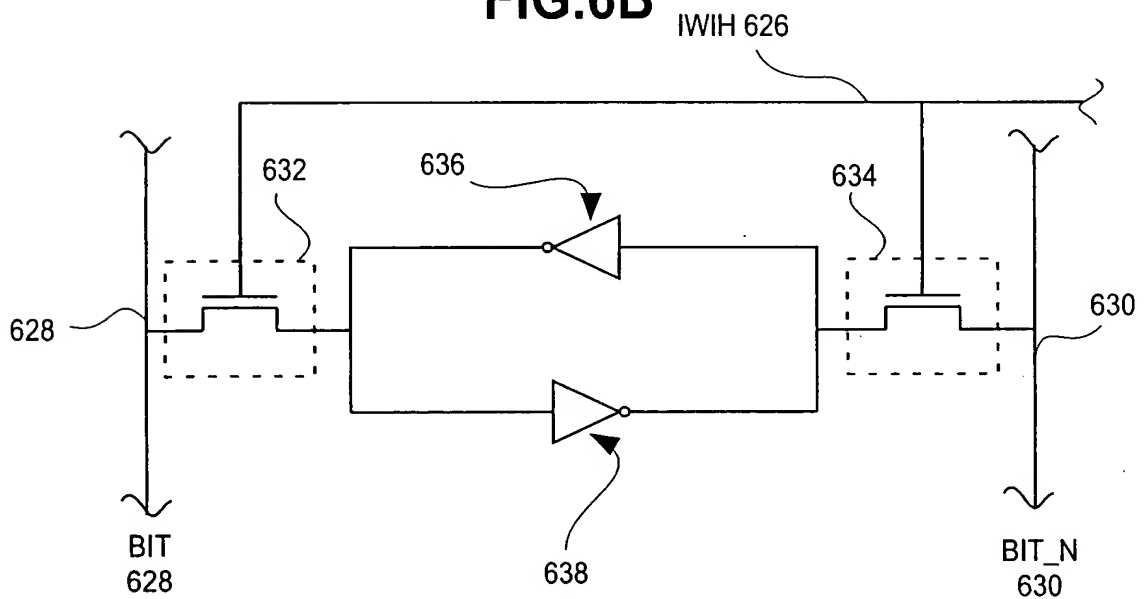


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**FIG.6A**

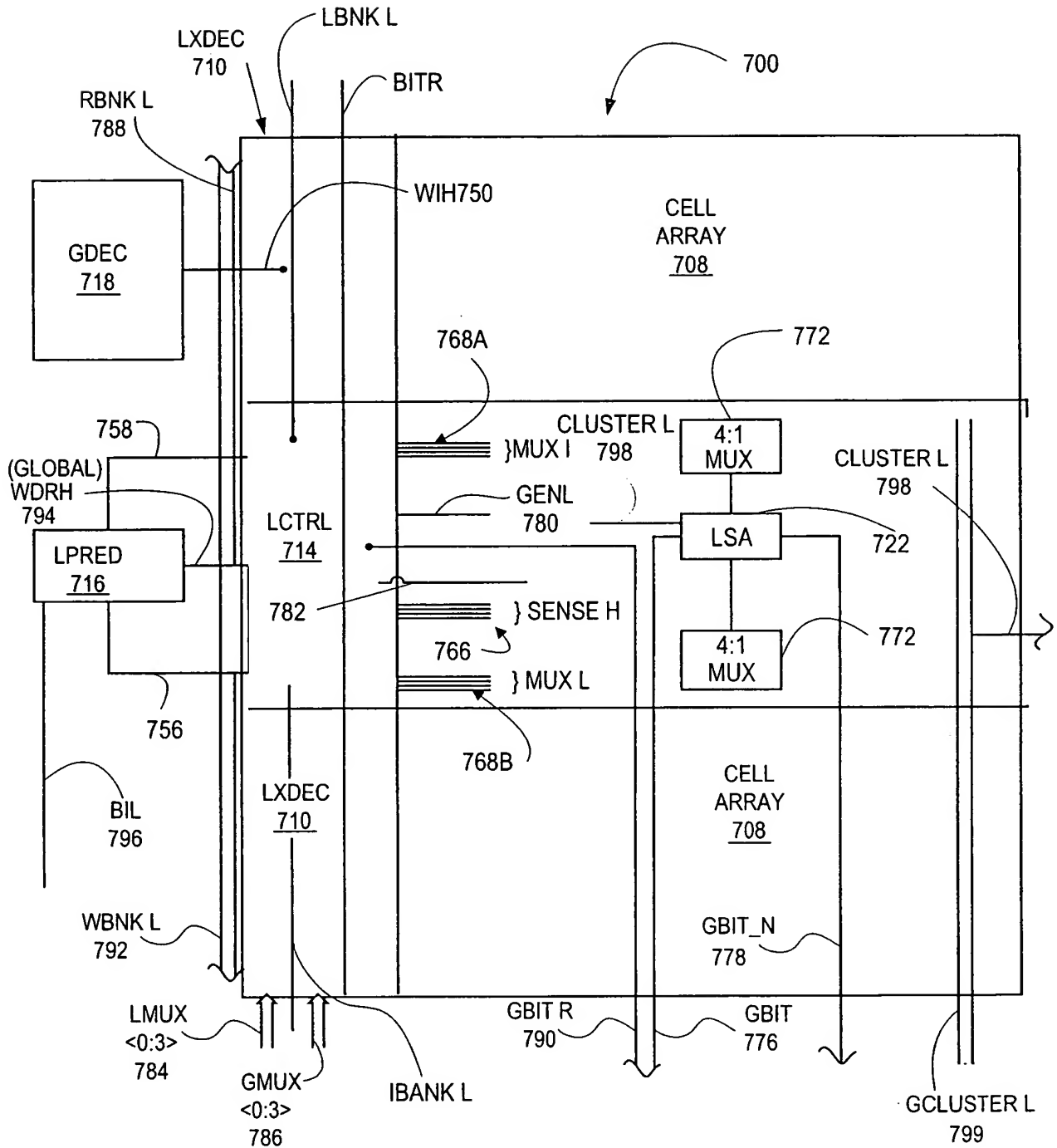


**FIG.6B**



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FIG. 7

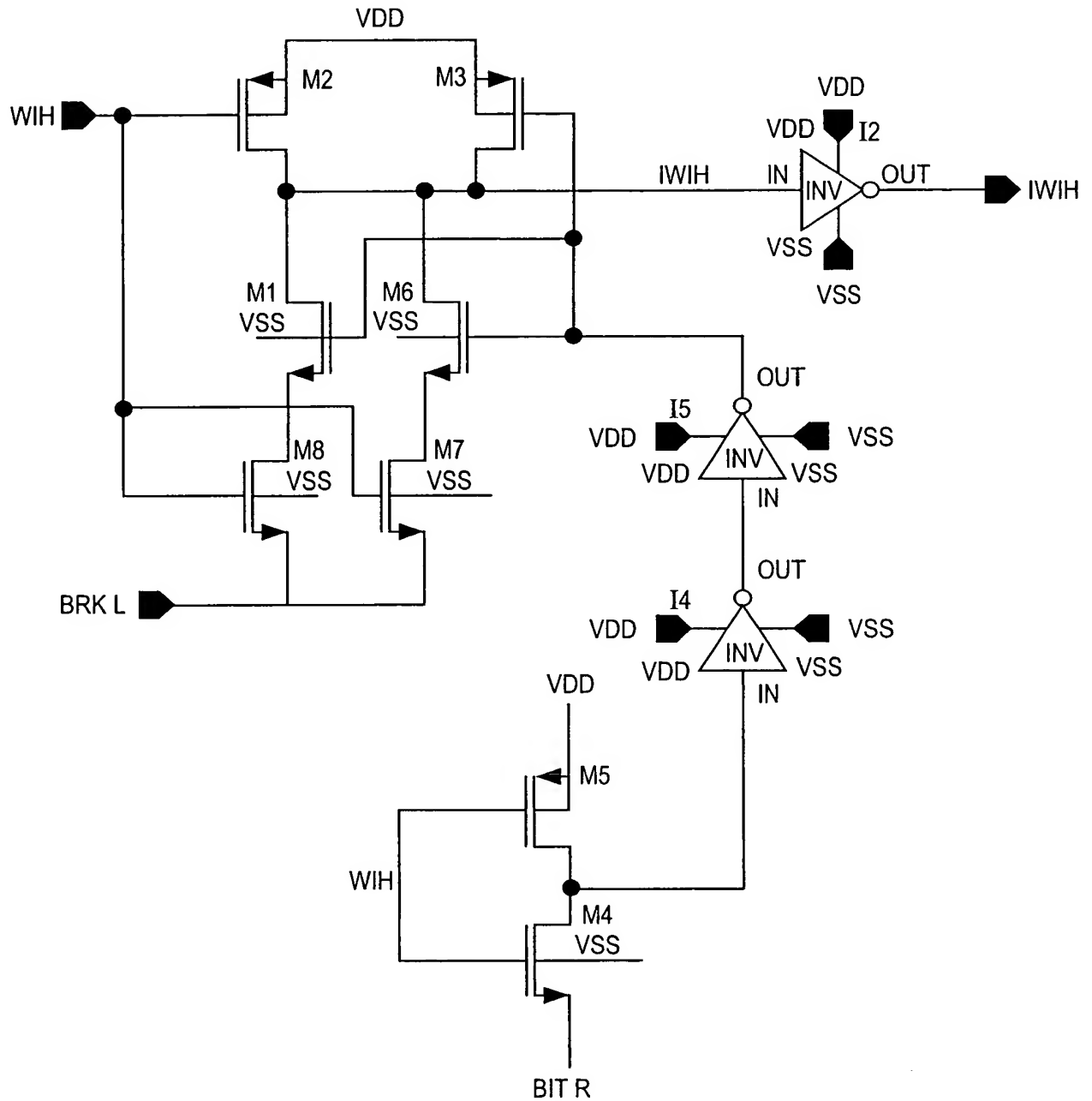






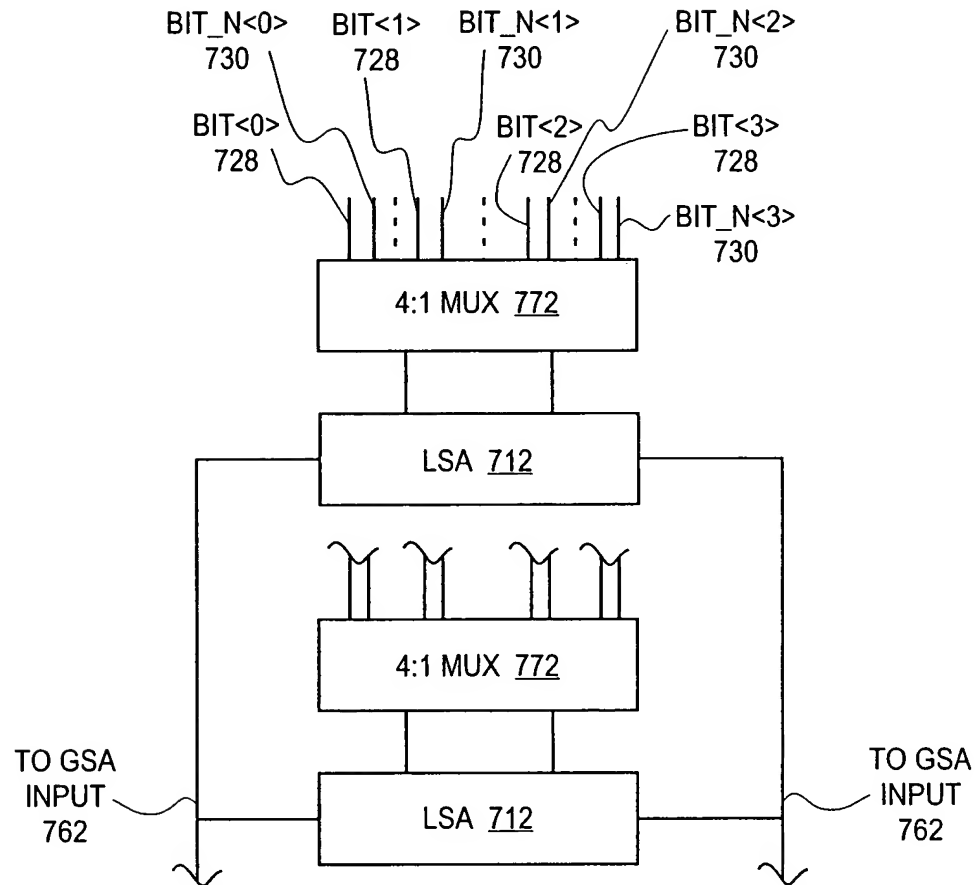
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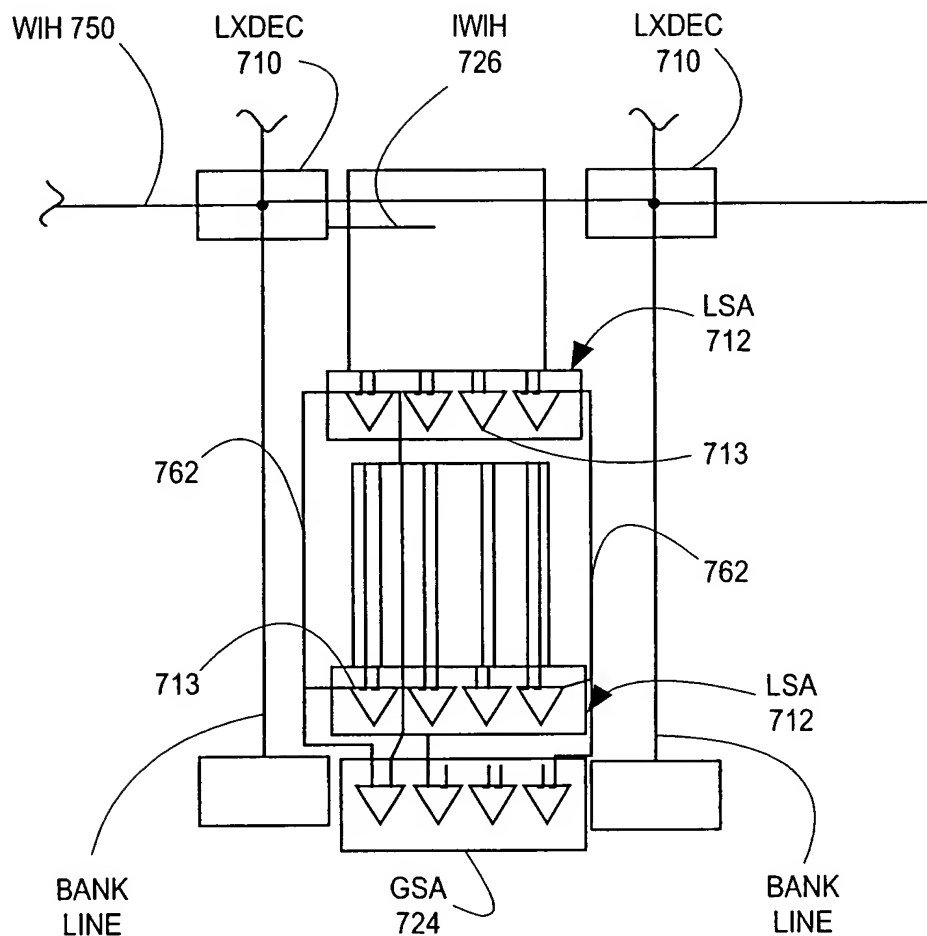
FIG. 9



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FIG. 10

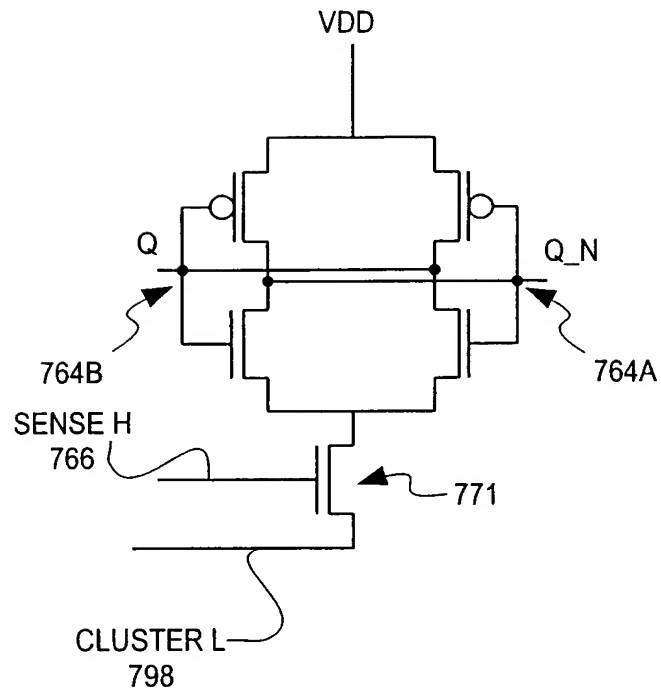




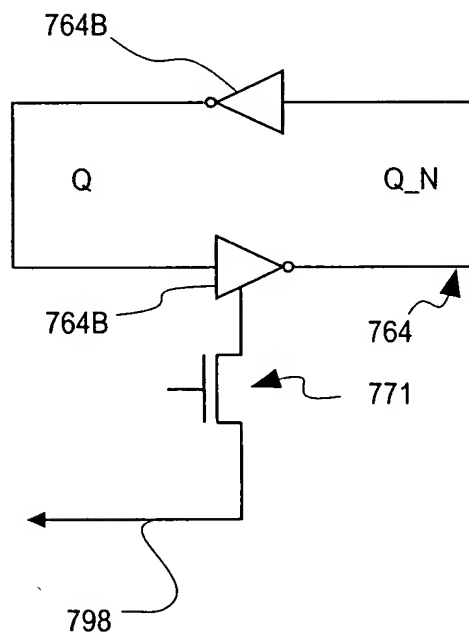
The schematic diagram illustrates a sense amplifier circuit. At the top, a block labeled "4:1 MUX + PRECHARGE" (772) receives inputs from "MUX L 768A" (three lines) and "BIT\_N 730" (four lines, labeled 774). The output of the MUX block is connected to a horizontal line. This line is connected to the input of a differential pair of transistors, labeled "Q" and "Q\_N". The gates of these transistors are connected to a horizontal line labeled "GEN L 775". The sources of both transistors are connected to a common source node, which is connected to a horizontal line labeled "GBIT 766". The drains of the transistors are connected to a horizontal line labeled "SENSE H X 4 766". The output of the differential pair is connected to a horizontal line labeled "CLUSTER L 798". The output of the cluster is connected to a horizontal line labeled "GBIT\_N 778". The output of the cluster is also connected to a horizontal line labeled "770". The output of the cluster is also connected to a horizontal line labeled "771". The output of the cluster is also connected to a horizontal line labeled "764B". The output of the cluster is also connected to a horizontal line labeled "764".

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**FIG. 12B**

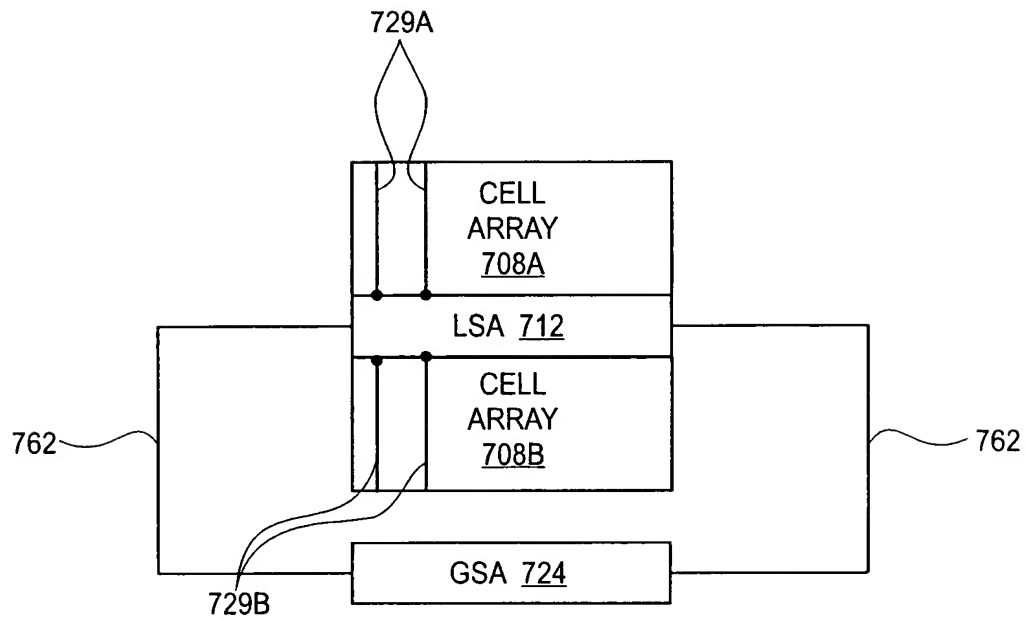


**FIG. 12C**



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FIG. 13



The detailed circuit diagram shows two multiplexers, MUX L<0> and MUX L<1>, each receiving inputs from BIT 728 and BIT\_N 730 through transistors 773A, 773B, and 773C. The outputs of these multiplexers are connected to a latch circuit consisting of cross-coupled inverters 764A and 764B, which also receive global bit signals GBIT and GBIT\_N through transistors 770.



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FIG. 15

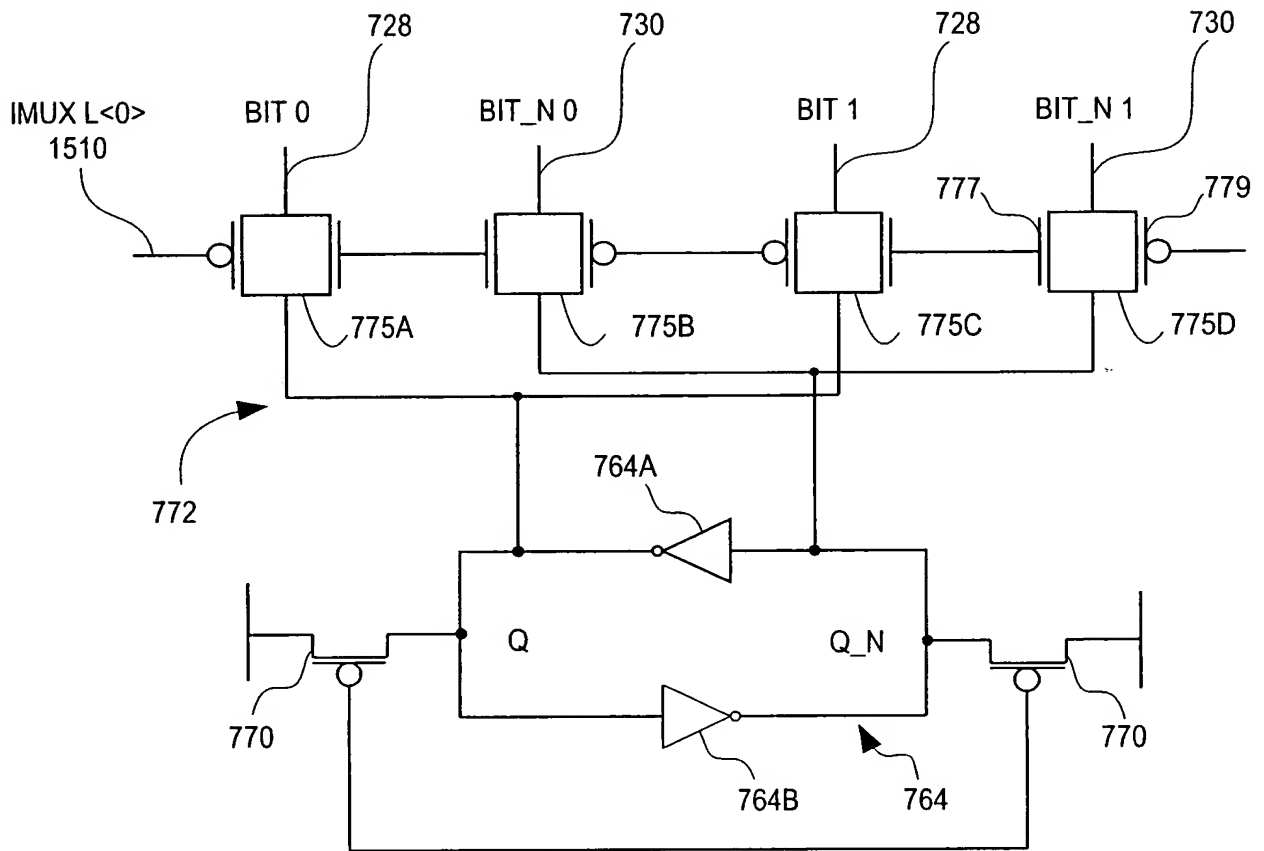
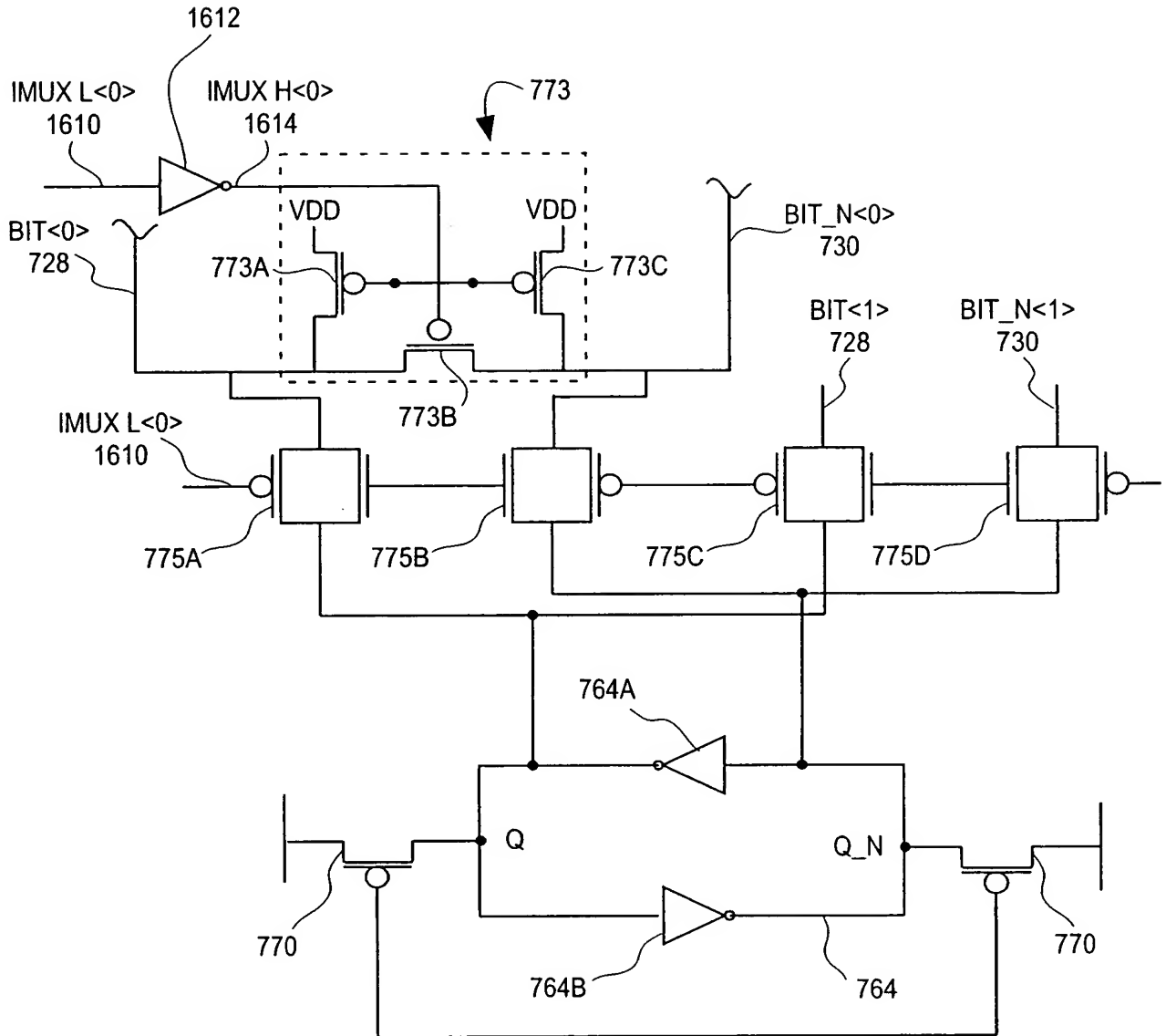
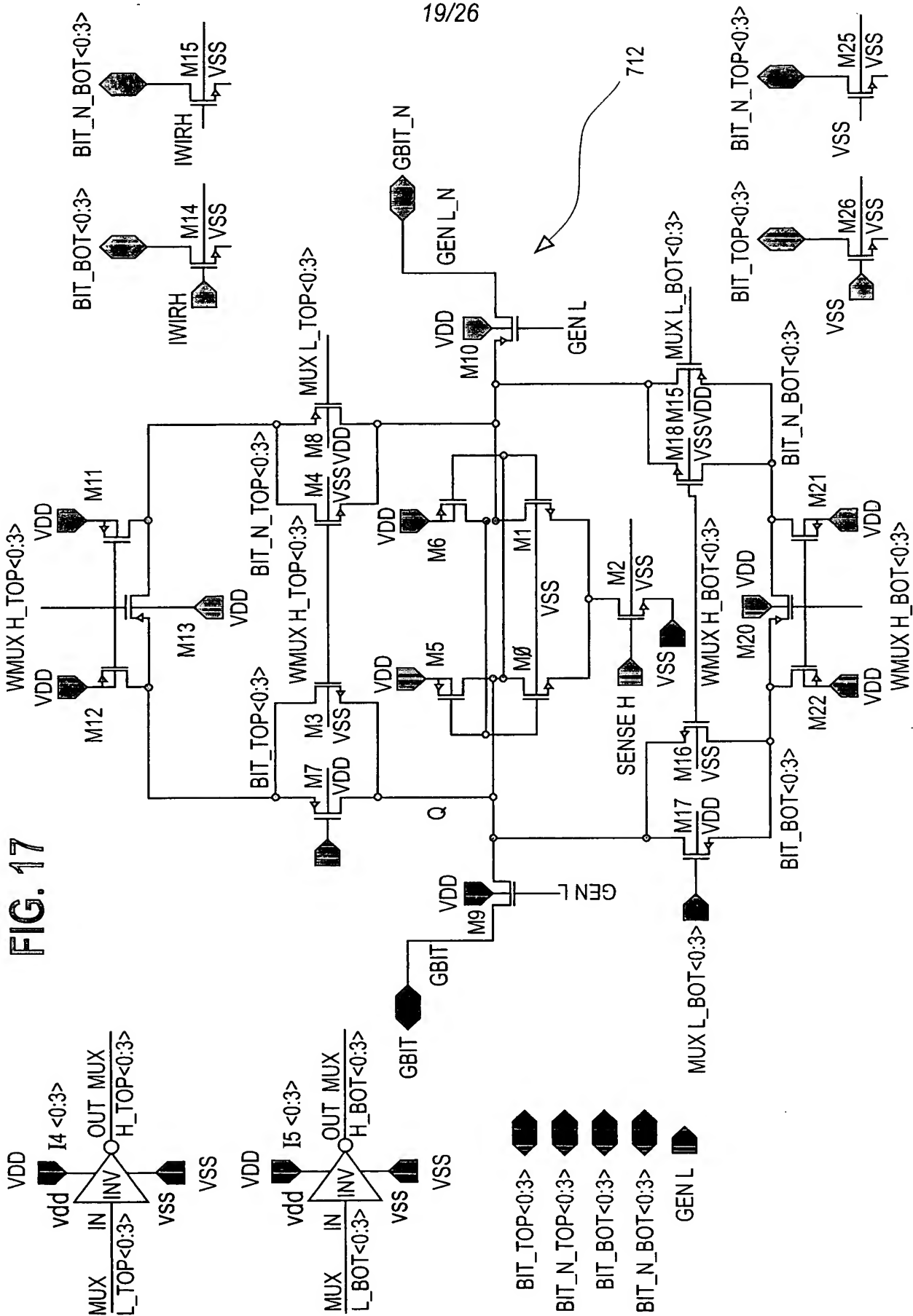


FIG. 16



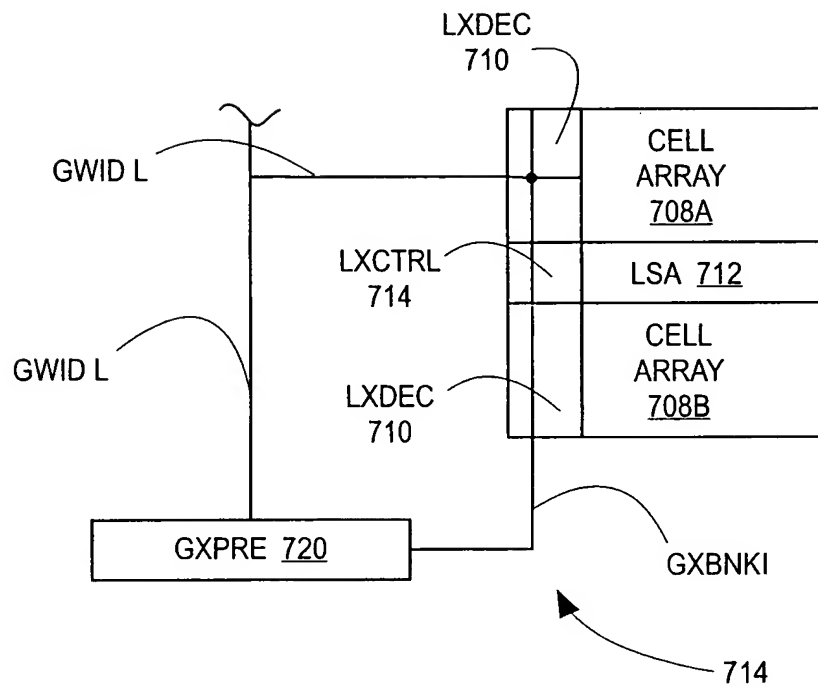
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FIG. 17



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FIG. 18



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FIG. 19

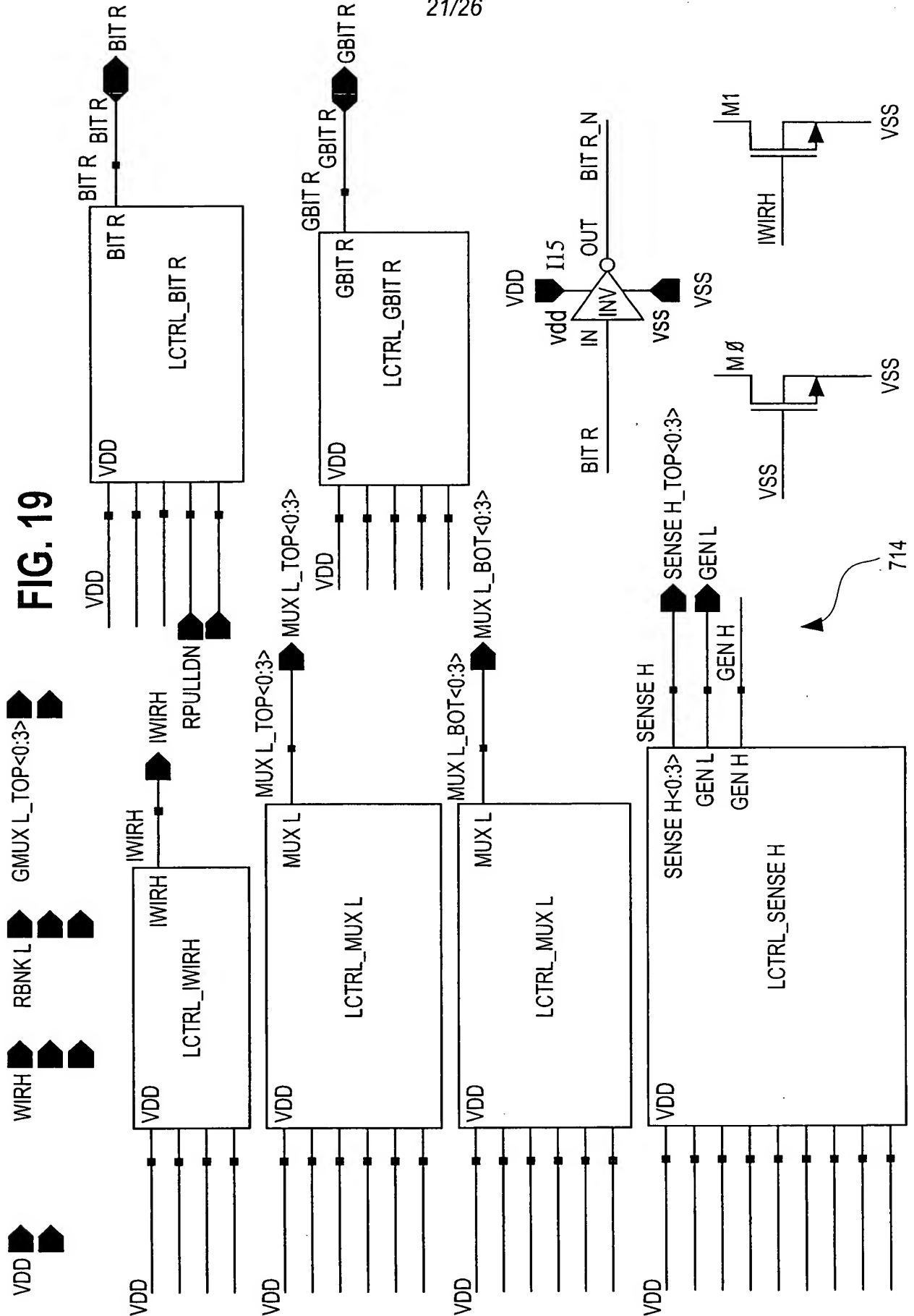


FIG. 20

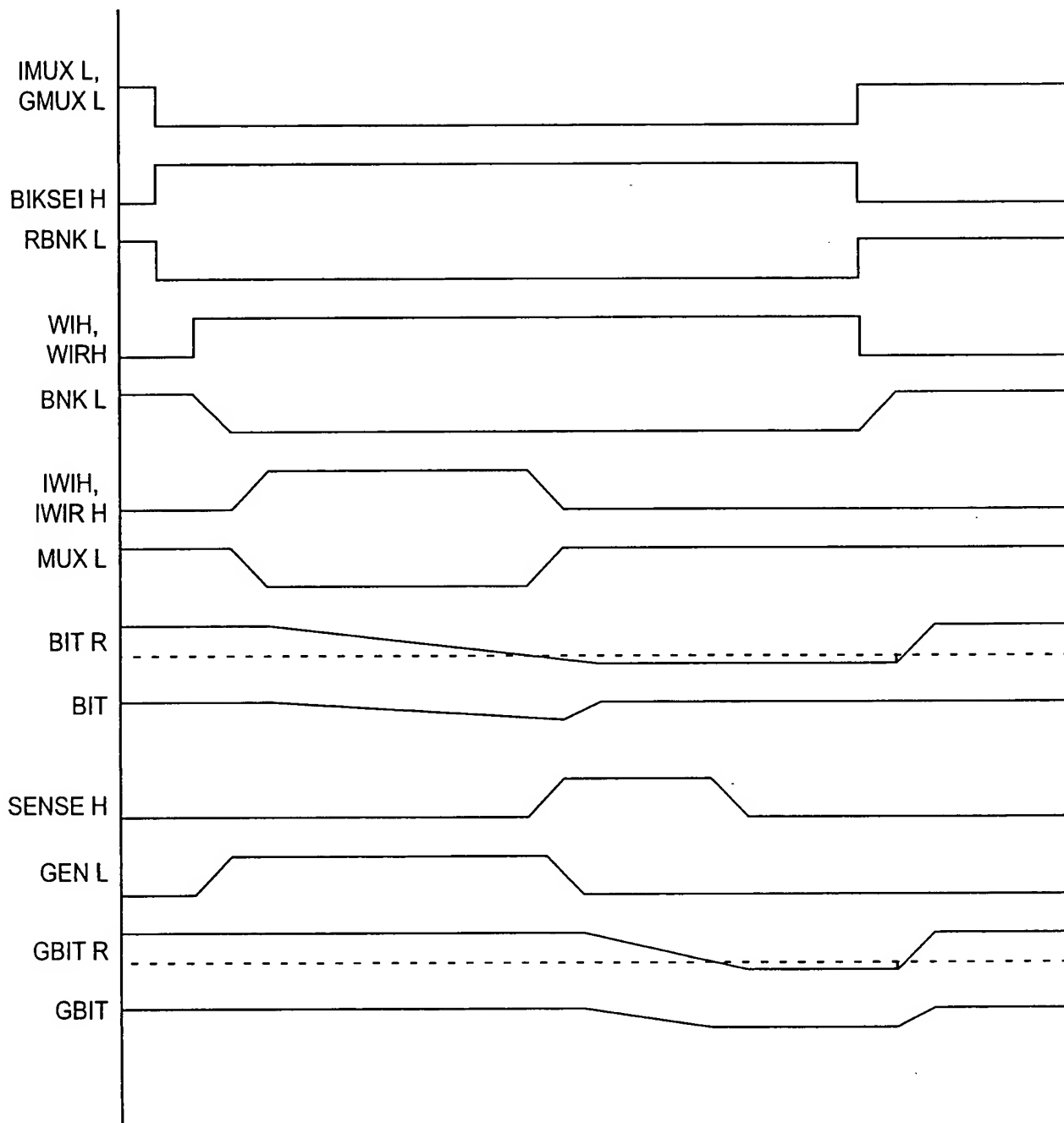
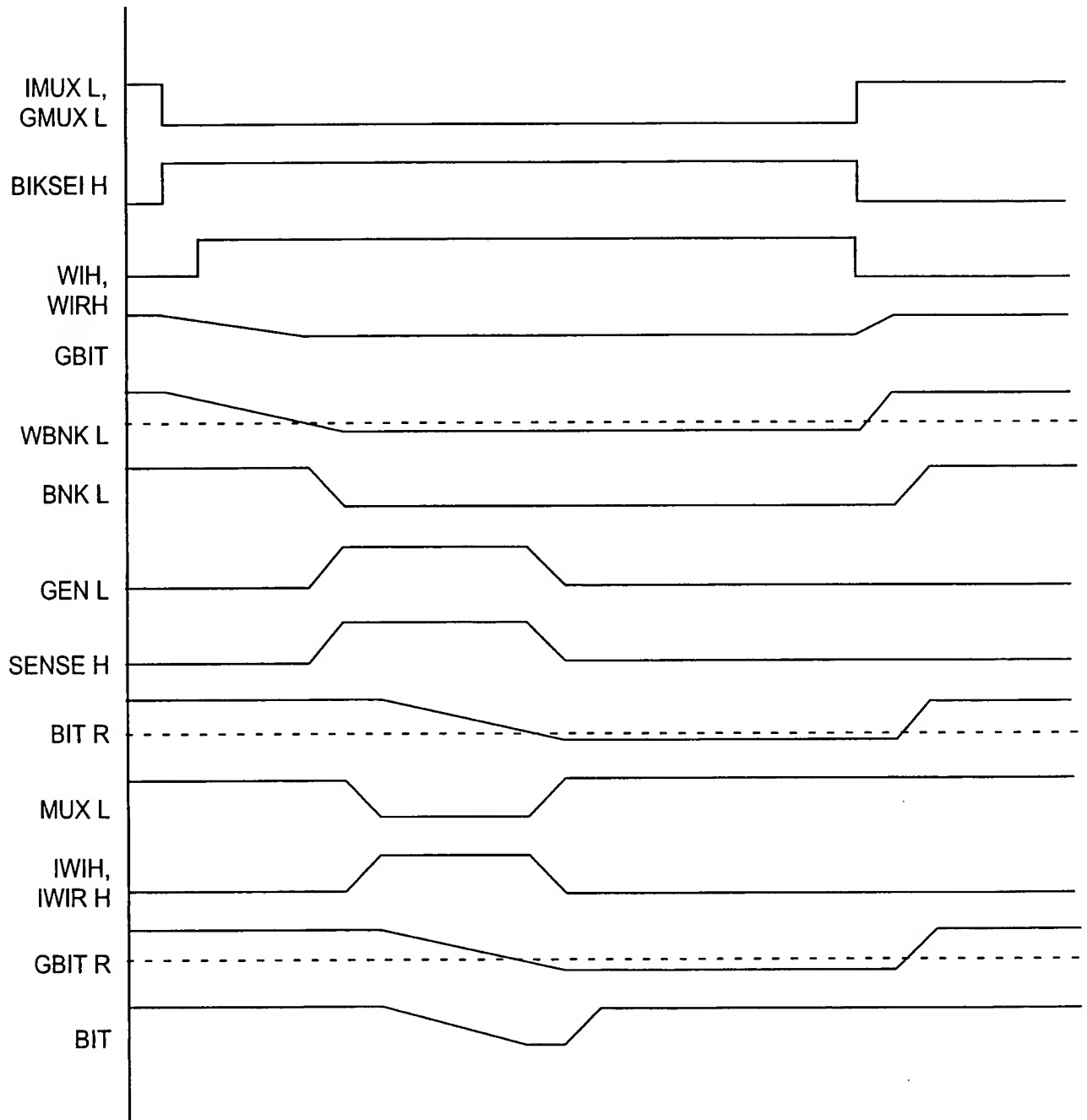


FIG. 21



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FIG. 22A

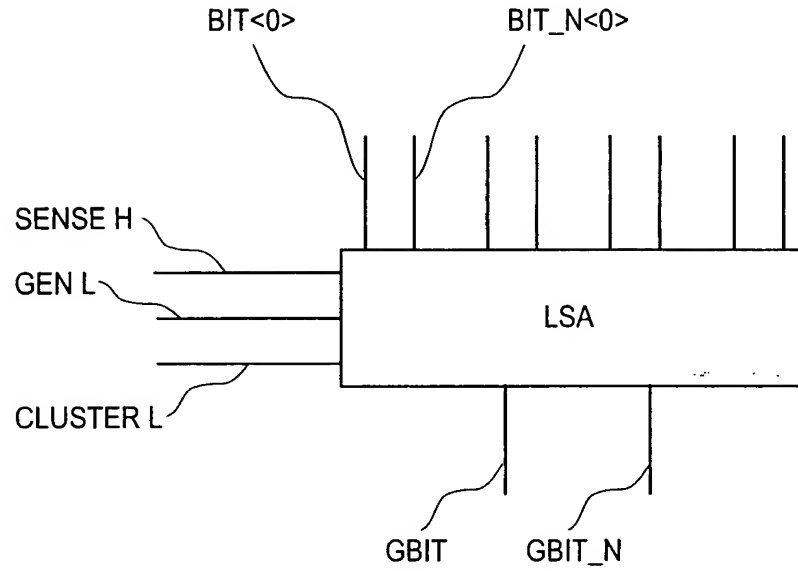


FIG. 22B

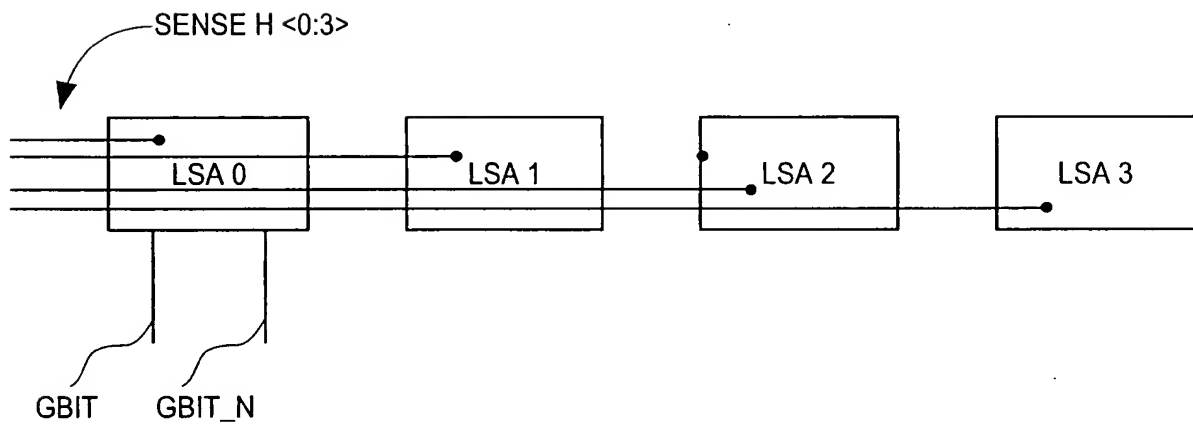




Figure 1 is a block diagram of a multi-processor system. It features a 'LOCAL CLUSTER' on the left, which contains eight processors labeled 'LSA 0' through 'LSA 7'. A signal 'SENSE H <0:3>' is shown entering the local cluster. To the right of the local cluster is a 'GCTRL' (Global Control) block. Further right is another 'LOCAL CLUSTER' containing processors 'LSA 4' through 'LSA 7'. A signal 'CLUSTER L' is shown between the two clusters. At the bottom, there are two signal lines labeled 'GBIT' and 'GBIT\_N'.

FIG. 23

